AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for transferring data between blocks in a design during simulation, comprising:

determining a first buffer size in response to specification of a vector input port of a first high-level block of the design;

determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design;

co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware-implemented block implements the first high-level block in the design simulated in a high-level modeling system (HLMS);

transferring a first vector of data values received by the first high-level block at the vector input port to the first hardware-implemented block via a single call to a first function provided by an interface that couples the HLMS to the first hardware-implemented block;

wherein the first vector of data values fills the first buffer size;

co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements the second high-level block in the design simulated in the HLMS;

accumulating a plurality of scalar data values received at the scalar input port in a second vector of data values that fills the second buffer size, by the second high-level block; and

transferring the second vector of data values from the second high-level block to the hardware-implemented block via a single call to the first function of the interface that couples the HLMS to the second hardware-implemented block.

2. (Currently Amended) The method of claim 1, further comprising:

simulating operation of a third high-level block in the design; and

transferring [[a]] the first vector of data values from the third high-level block to the vector input port of the first high-level block.

3. (Currently Amended) The method of claim 1, further comprising:

co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware-implemented block implements a third high-level block in the design simulated in the HLMS; and

transferring [[a]] the first vector of data values from the third high-level block to the vector input port of the first high-level block.

4. (Previously Presented) The method of claim 1, further comprising transferring a third vector of data values received by the interface from the first hardware-implemented block, to the first high-level block in response to a single call to a second function provided by the interface and invoked by the first high-level block.

5. (Previously Presented) The method of claim 4, further comprising:

simulating operation of a third high-level block in the design in the HLMS; and

transferring the third vector of data values from the first high-level block to the third high-level block.

6. (Currently Amended) The method of claim 4, further comprising:

co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware-implemented block implements a third high-level block in the design simulated in the HLMS; and

transferring the ~~second~~ third vector of data values from the first high-level block to the third high-level block.

7. (Previously Presented) The method of claim 4, wherein the hardware co-simulation platform includes a field programmable gate array (FPGA), and the method further comprises:

establishing a first buffer of the first buffer size and a second buffer of the second buffer size on the FPGA; and

wherein the transferring the first vector and transferring the second vector include temporarily storing the first vector and the second vector in the first and second buffers.

8. (Previously Presented) The method of claim 7, wherein the determining the first buffer size comprises determining an associated size of the vector input port, wherein the required size of the buffer is equal to the size of the vector.

9. (Previously Presented) The method of claim 7, wherein the determining the first buffer size comprises determining the first buffer size as a function of a value of a user-provided configuration parameter.

10. (Original) The method of claim 9, wherein the configuration parameter is associated a buffer-size compilation option of the HLMS.

11. (Original) The method of claim 7, wherein one or more input/output ports each has an associated configuration parameter value.

12. (Previously Presented) The method of claim 7, further comprising:

estimating FPGA resources available for buffers; and

selecting the first and second buffer sizes as a function of the estimated available resources.

Claim 13. (Cancelled)

14. (Previously Presented) The method of claim 1, further comprising:

simulating operation of a third high-level block in the design in a high-level modeling system (HLMS); and

transferring the plurality of scalar values from the third high-level block to the second high-level block.

15. (Currently Amended) The method of claim 1 [[13]], further comprising:

co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware-implemented block implements a third high-level block in the design simulated in the HLMS; and

transferring the plurality of scalar values from the third high-level block to the second high-level block.

16. (Currently Amended) The method of claim 1 [[13]], further comprising:

simulating operation of a third high-level block in the design in a high-level modeling system (HLMS); and

outputting a sequence of scalar values from a vector of data received by the second high-level block from the first hardware-implemented block to the third high-level block.

17. (Currently Amended) The method of claim 1 [[13]], further comprising:

co-simulating a third hardware-implemented block on a hardware co-simulation platform, wherein the third hardware-implemented block implements a third high-level block in the design; and

outputting a sequence of scalar values from a vector of data received by the second high-level block to the third high-level block.

Claims 18-22. (Cancelled)

23. (Previously Presented) An apparatus for transferring data between blocks in a design during simulation, comprising:

means for determining a first buffer size in response to specification of a vector input port of a first high-level block of the design;

means for determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design;

means for co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware-implemented block implements the first high-level block in the design simulated in a high-level modeling system (HLMS);

means for transferring a first frame of data received by the first high-level block at the vector input port to the first hardware-implemented block via a single call to a first function provided by an interface that couples the HLMS to the first hardware-implemented block;

wherein the first vector of data values fills the first buffer size;

means for co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware-implemented block implements the second high-level block in the design simulated in the HLMS;

means for accumulating a plurality of scalar data values received at the scalar input port in a second vector of data values that fills the second buffer size, by the second high-level block; and

means for transferring the second vector of data values from the second high-level block to the hardware-implemented block via a single call to the first function of the interface that couples the HLMS to the second hardware-implemented block.

Claim 24. (Cancelled)